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Design, Modeling of Ga-As based MESFET for SRAM Cell

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***Abstract*: The main attention in the area of technology is given to the low power SRAM (Static random Access Memory).GaAs SRAM have been developed with great efforts which include its many advantages such as reduced power consumption and temperature tolerance. There are many limitations of conventional cell which are overcome by the design of new cell which is used to simulate SRAM. The structure of MESFET and the limitations are discussed in the paper. Further, a code in silvaco is run and simulated and the result analysis is done using tony plots.**

***Keywords:* GaAs MESFET, SRAM, memory cells, leakage current, transistors.**

I. INTRODUCTION

GaAs Large Scale Integrated technology has played a very important and crucial role in the area of electronics which has been growing at a very fast speed. The main attention in this area of technology is given to the low power SRAM (Static Random Access Memory) [1-2]. GaAs SRAM have been developed with great efforts which include its many advantages such as reduced power consumption and temperature tolerance. GaAs microprocessors of very high speed include the high-speed GaAs chips and memories in which on-chip memory is used in very small amount so that high speed benefits can be obtained [3-4].

The main difference between the MOSFET and MESFET is that the insulator is not present under the gate. The structure of MESFET is shown in figure 1. When the MESFET is in transistor mode, the gate should be biased so that the underlying channel is controlled in reverse biased. The extent of the gate metal is the most important aspect in the MESFET design [5]. The ability of the MESFET handling the current is improved due to the lateral elongation of the gate. But the effect of the transmission line limits the phase shift of the gate [6-7].

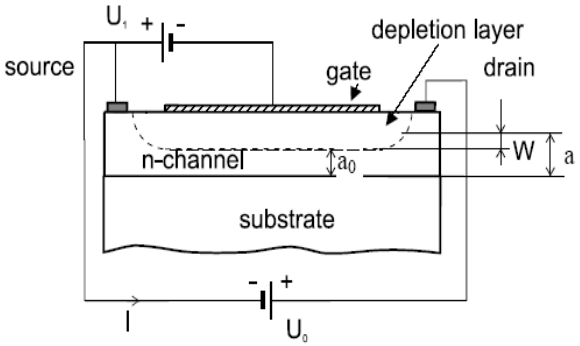

Fig. 1. Structure of MESFET

SRAM is used to implement the conventional memory cell which used six transistors which had several limitations. The problems in conventional cells is shown in figure 2. There are many limitations in the conventional cell which include the capacitive coupling of the bit lines and the nodes of the cell, injection of current into the cell through access transistor and the generation of destructive readout [8]. Because of these limitations, the conventional cells cannot be implemented on the structures of SRAM GaAs. The (i) includes the capacitive coupling of the nodes. The (ii) includes injection through gate-source diode [9].

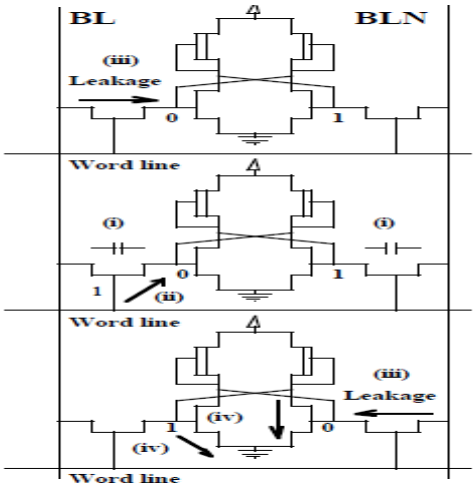

Fig. 2. Limitations of conventional memory cell

The leakage current in the MESFET flows in the cells which are not selected and in the "low" node. The leakage current is not defined by the individual transistors but is the sum of the combined data stored in the columns of the columns of the transistor where the leakage current flows in the non-selected cells and in the memory cells [10]. This is the (iii) limitation of the conventional cell as shown in the figure above. When the leakage current flowing from drain to source is increased in the enhancement FET then the Schottky current flowing from gate to source is increased in the succeeding stage of the enhancement FET. The internal node level of "high" is reduced which includes the (iv) limitation of the conventional cell [11]. The increase in the leakage current also affects the working of the circuit of SRAM GaAs which further disturbs the memory cell stability in case there is variation in the temperature. The memory cells containing the access transistors are all affected by the certain limitations of the conventional memory cell as described above which makes them unsuitable for low power SRAM GaAs structures [12].

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II. DESIGN OF SRAM CELL

The high-speed cell for the simulation of SRAM cell is shown in figure 3. This cell is the mixture of advantages of mirror cells and conventional cells [13]. The structure of the cell consists of MESFET transistors, devices and diodes.

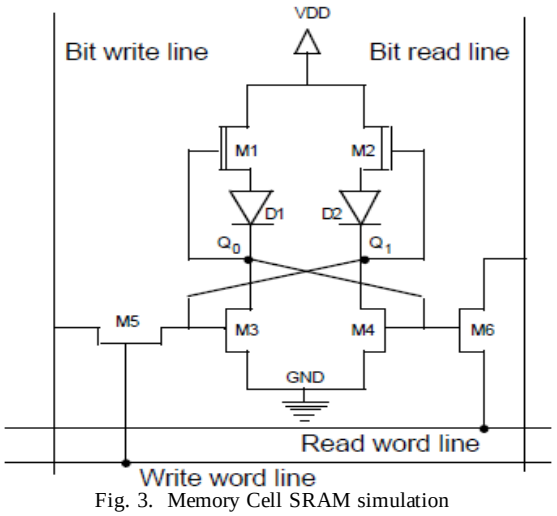

Fig. 3. Memory Cell SRAM simulation

M1 and M2 are the depletion transistors in which the source-gate biasing is done. The transistors are used to reduce the threshold current which results in reduced power dissipation from the cell. D1and D2 are the two diodes with the help of which back biasing is done. It is necessary to maintain the high level in the node which is done by considering the ime requirements and reduction in the power [14-15]. The combination of the diodes and depletion transistors should be such that there is compensation of leakage current and Schottky current in order to achieve reduced power consumption. M1-D1 forms the current source which is weak and therefore large currents must be provided by it. This current should be greater than the sum of the currents of gate to source M4 and M6 and the threshold current flowing from source to drain in M3 [16]. Similarly, the M2-D2 current source should provide the currents larger than the threshold current in M4 and M5 in addition to the Schottky current in gate of M3 [17]. The subthreshold current in the depletion transistors M4 and m5 is given as

$$I_{sub} = C1.W.n_o(1-e^{-Uds})/L \quad (1)$$

The Schottky current in M3 gate is given as

$$I_{Sh} = W.l\,(C2.e^{-Uds})\,e^{U} \quad (2)$$

Where,

$$C1 = 2.L_{B.}q.D_n$$
$$C2 = q.N_{D.}V$$

$D_n$is diffusion constant
n_0 is concentration of minority carriers at equilibrium
N_D is doping concentration.
The saturation current of the transistor is given by

$$I_{ds} = \beta(V_{gs}-V_T)^2\,(1+\lambda V_{ds})\,tanh(\alpha V_{ds}) \quad (3)$$

III. BASIC CIRCUIT

The basic circuit includes the input registers, memory array, sense amplifier, output registers, bit lines and input output circuitry [17]. The block diagram is shown in figure 4. The different parts of the block diagram play crucial role in the simulation of SRAM.

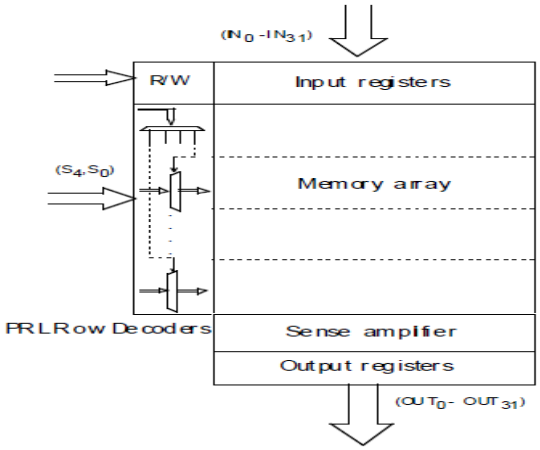

Fig. 4. Block Diagram

The access time mainly contains the word line selection time which is responsible for the time delay between the word line and the address input. This selection time is reduced by applying the method of selecting the rows in the circuit. A memory array is divided into different address signals and blocks which are divided into two main groups. These groups are used for block selection and row selection. PRL decoders are used for decoding the block for reducing the power dissipation. On selection of one block, the other blocks are deactivated so that they have low outputs and therefore are put to ground. Reducing the RC delay is the requirement of technology and therefore this method has a very large significance in reducing the time delay and consumption of power. This also helps in reducing the array current so that the lowering of the high level can be prevented. There is decrease in the high level with increase in temperature by the Schottky diodes present in decoder circuit. The power rail method of decoding is used to improve the operational margin. The sense amplifiers are used so that the transient time in the read operation can be reduced [18]. The voltage levels in the sense amplifiers are stored in registers contained at the output stage providing a good fanout.

IV. SENSE AMPLIFIER

The sense amplifier is used at no reading operation so that the power consumption is low. Figure 5 shows the PRL sense amplifier. The sense amplifier consists of inverter and NOR gates. There is buffering of the read signal during the read operation through which the power is supplied to NOR SR latch. The charge leakage is avoided in the transistors M4 and M5 to the nodes which are uncharged [19].The positive feedback is provided through this method which allows rapid switching. This is useful when the difference between the voltages at the output node is small.

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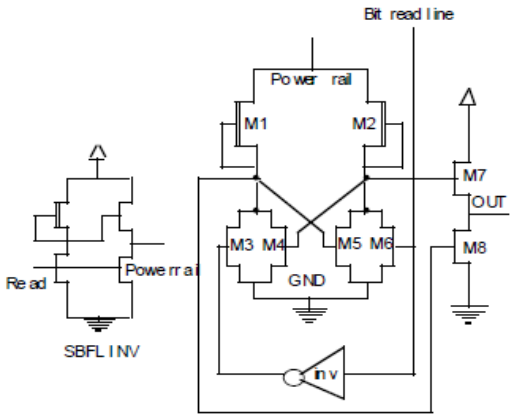

Fig. 5. Sense Amplifier

Direct read signals are connected to M6 and complimentry signals are connected to M3. The complimentry signal is generated by the inverter used with NOR gate for the operation of sense amplifier. The buffering of the voltage levels is done internally by the output of the sense amplifier which offers maximum gain to operate at the appropriate voltage levels [20].

V. SILVACO CODE FOR GA AS MESFET

```
goathena
# GaAs MESFET fabrication and analysis usingDevEdit
line x loc =-1.5 spac=0.2
line x loc =-.7 spac=0.1
line x loc =-.5  spac=0.05
line  x loc =0.0   spac=0.1
line x loc =0.5   spac=0.05
line x loc=1.5 spac=0.2
#line y  loc =0.00 spac=0.02
liney loc= 2.00  spac=0.5
#Init gaas c.beryllium  = 1.0e13 orient= 100 space.mult=1
Implant beryllium energy = 100 dose = 2e11
Implant silicon energy=100 dose = 1e12
Diffuse time= 10 temp = 850

# deposi and patterngate metal
Deposit titanium thick =.3 divisions = 10
etch titanium right p1.x =0.5
etch titanium left  p1.x =-0.5
deposit oxide thick =0.35 divisions=8
etch oxide thick=.4
# perform source/drain implant
implant silicon energy=50 dose=1e13
diff time=10 temp=850
# deposit ohmic metal
deposit aluminum thick =.2 divisions =4
etch aluminum  start x =-1 y= 10
etch cont       x=-1 y = -10
etch cont     x=1 y=-10
etch done   x=1 y=10
#electrode name = source  x=-1.4
electrode name = drain x=1.4
electrode name = gate x=0.0
structure outfile=mesfetex01_0.str
tonyplot mesfetex01_0.str  -set mesfetex01_0.set
go atlas
# set work function for gate
contact name= gate work =4.87
# specify lifetimes in GaAs and models
Material material=GaAS taun0 =1.e-8 taup0=1.e-8
models conmobfldmob srhoptr print
#Begin solution
Method newton trap
solve vdrain = 0.1
# Ramp gate and log results
log outf= mesfetex01.log master
solve vgate= 0.0 vstep= -0.1 vfinal= -3 name= gate
extract initinfile="mesfetdesign.log"
 extract
 name="vt"
(xintercept(maxslope(curve((v ."gate"),(i ."drain")))))
save outfile = mesfetex01_1.str
tonyplot mesfetex01.log
quit
```

VI. SIMULATION AND RESULTS

The design was made and analyzed on SILVACO. Figure 6 shows tonyplot of fabricated MESFET device in simulation. MESFET should be biased such that it should not have forward conducting diode instead of depletion zone of reversed biased which is controlling the channel underlying. The gate metal extent over switching zone is critical aspect of design. Figure 7 shows the voltage and current characteristics in silvacoafter simulation. The threshold voltage V_{th}= -0.459.

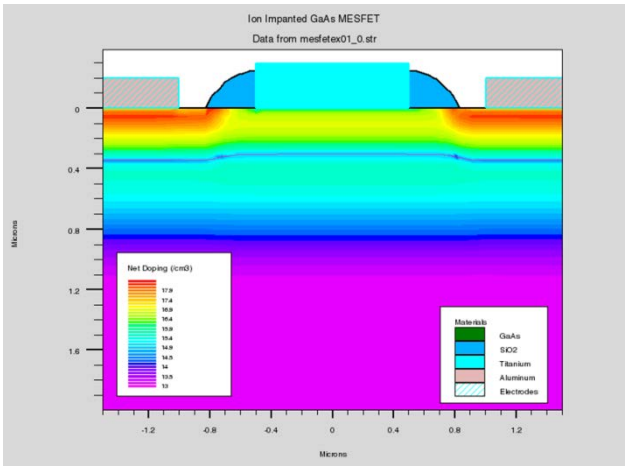

Fig. 6. Tonyplot for MESFET

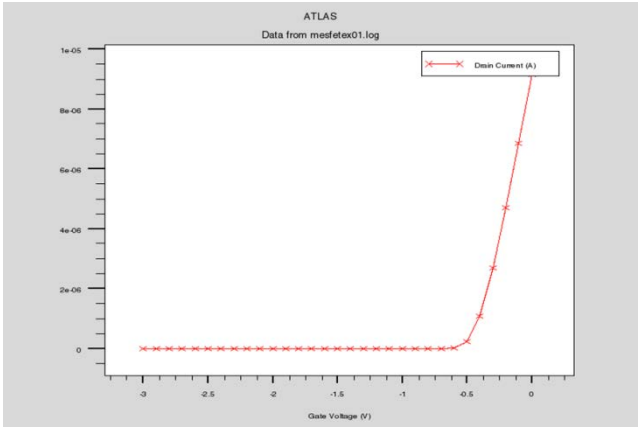

Fig. 7. V-I characteristics of MESFET

VII. CONCLUSION

In this paper, GaAs MESFET is discussed because of many limitations in the conventional cell. All the limitations are discussed in detail and shown in the diagram. This gave rise to the new cell which overcame all the disadvantages of the conventional cell and which could be implemented and simulated for SRAMs. The design of the SRAM cell is discussed in detail which includes the read and write operations. Further the basic circuit diagram of the cell simulating SRAM has been discussed including all its components such as sense amplifier which is elaborated in detail. Silvaco is used to implement the results of MESFET showing its voltage and current characteristics. The code is given. In the end of the paper, the tonyplots for the MESFET characteristics is shown.

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